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Transparent AMOLED Display Driven by Split Oxide TFT Backplane

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Abstract

We have developed stable and high performance etch-stopper (E/S) a-IGZO TFT by using split oxide semiconductor layer. The a-IGZO TFTs exhibit high mobility over 70 cm^2/Vs and extremely stable under positive bias temperature stress. In this work we demonstrated a 4 inch transparent AMOLED using oxide TFT backplane with split active layer, where the gate driver is integrated.

Author Keywords

Split; oxide; thin-film transistor (TFT); High mobility; transparent AMOLED

1. Introduction

There is increasing interest in high mobility thin-film transistor (TFT) for high resolution and large area active-matrix organic light-emitting diode (AMOLED) displays. High resolution AMOLED displays based on oxide TFT backplane have been receiving increased attention recently [1-2]. The TFT backplane for OLEDs can be realized with low-temperature polycrystalline silicon (LTPS) or transparent amorphous oxide semiconductors (TAOS) because of the high mobility of these materials. However, amorphous-silicon (a-Si:H) TFTs have an inherent issue of threshold-voltage (V_{TH}) shift during OLED operations so that cannot be used for AMOLED display. Conventionally, the p-channel LTPS TFT backplanes have been widely used for smartphone AMOLED display, due to their high hole mobility (>100cm^2/Vs). However, their drawbacks are the poor material uniformity and high process temperature over 450℃ [3].

Transparent amorphous-oxide-semiconductor (TAOS), particularly amorphous-indium-gallium-zinc-oxide (a-IGZO), has attracted considerable attention for applications in large-size, transparent AMOLED displays because it yields high device performance even deposited at low temperature. Recently, a-IGZO TFT backplane is being used for AMOLED TV, but the mobility should be further improved for its wide application. Therefore, high mobility a-IGZO TFT is getting more attention recently [4-5]. Before we reported the split TFTs exhibiting high mobility over 70 cm^2/Vs with excellent bias and temperature stabilities. Here we demonstrated a 4-inch transparent AMOLED with integrated gate driver.

2. Experimental

We have fabricated the inverted staggered a-IGZO TFTs on glass substrate with the etch-stopper (E/S) structure as shown in Fig. 1a. The E/S TFT structure with standard (STD) and split active oxide semiconductor (Split) are shown in Fig. 1(b) and 1(c), with corresponding optical images in Fig. 1(d) and 1(e), respectively.[6] Fig. 1(c) shows a schematic diagram of TFT with divided active semiconductor layer with 2 μm of unit width. Note that the total width (WT) of all TFTs is fixed 100 μm with 1.5 μm space between active islands.

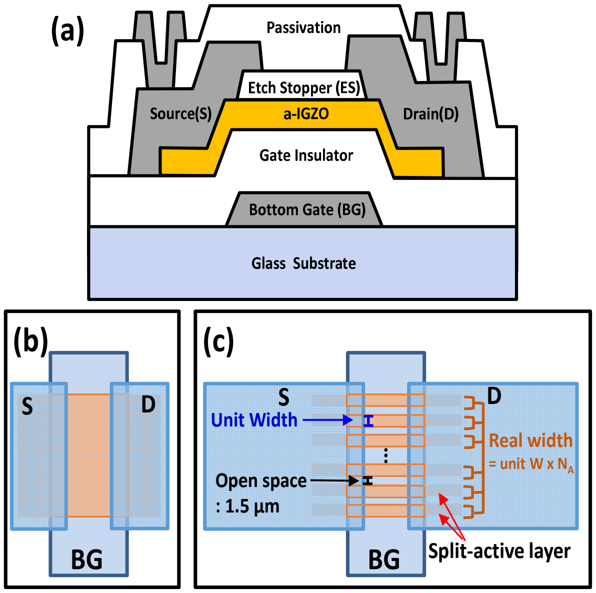

Figure 1. (a) Schematic cross-section of the a-IGZO TFTs with etch-stopper structures. Structures of the gate a-IGZO TFTs with (b) standard and (c) split active layer.

The TFTs are fabricated through etch-stopper (E/S) process as described elsewhere [6]. A 60-nm-thick Mo layer was deposited on a glass substrate by sputtering and then patterned for a bottom-gate (BG) electrode. Then, a SiNx and SiO2 double gate insulator was deposited through plasma-enhanced chemical vapor deposited (PECVD). This was followed by the consecutive deposition of a thin a-IGZO layer and a PECVD SiO2 E/S layer, without breaking vacuum, to ensure clean interface. E/S SiO2 layer was deposited by PECVD and patterned by dry etching for the split pattern as shown in Fig. 1(c). After this, a 150- nm Mo was deposited and patterned as the source/drain electrodes, followed by the deposition of PECVD SiO2 layer as the passivation layer. An IZO layer is deposited and patterned to form the pixel electrode, anode for OLED[7]. Then, to form the transparent OLED stack, 1,4,5,8,9,11-hexaazatriphenylene-hexacarbonitrile (HAT-CN) (20 nm) as a hole injection layer, N,N'–di(naphthalene-1-yl)-N,N'-diphenylbenzidine (NPB) (50 nm) as a hole transport layer, 4,4',4''-tris(carbazol-9-yl)-triphenylamine (TCTA) (5 nm) as an exciton blocking layer, TCTA:2,2',2''-(1,3,5-benzenetriyl)-tris-[1-phenyl-1-H-benzimidazole] (TPBi):12% tris(2-phenylpyridinato-C2,N)iridium(III) (Ir(ppy)3) (15 nm) as an emission layer, TPBi (45 nm) as an electron transport layer, and LiF (0.5 nm)/Al (1 nm)/Ag (22 nm) as a transparent cathode. Finally, the transparent AMOLED on TFT backplane was encapsulated with glass in a N_2 filled glove box.

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Fig. 2 shows that the schematic cross-section of one pixel. All electrical measurements were monitored by the Agilent 4156 C semiconductor parameter analyzer and carried out in dark and at room temperature. And, V_{TH} is defined as the V_{GS} corresponding to I_{DS}=W/L x10 pA. The field-effect mobility (μ_{FE}) is derived from the transconductance (g_M) with V_{DS}=0.1 V. The sub-threshold swing (SS) is taken as (d log (I_{DS})/d V_{GS})-1 of the range 10 pA$\leq I_{DS} \leq$100pA, with V_{DS} = 0.1 V.

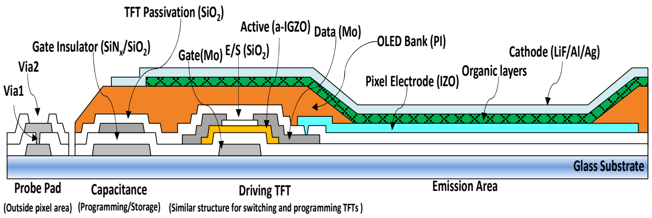

Figure 2. (a) Schematic cross-section of one pixel of a 4-inch transparent AMOLED display. The AMOLED display is demonstrated by using IGZO TFT backplane with split active layer and transparent OLED with an IZO/HAT-CN/NPB/TCTA/TCTA:TPBi:12% Ir(ppy)3/TPBi/LiF/Al/Ag.

3. Results and Discussion

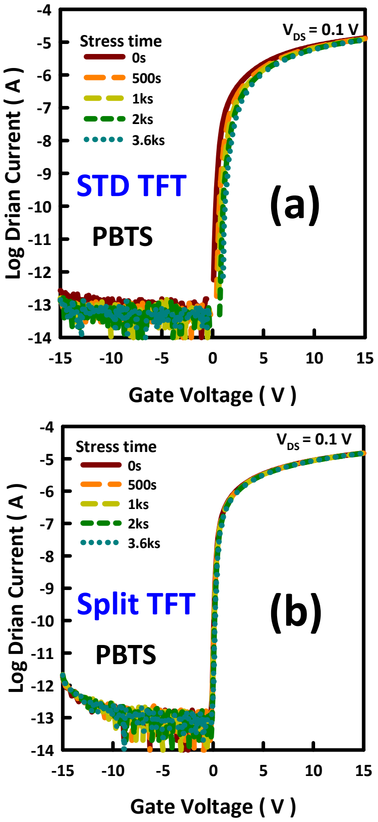

Figure 3. Device stability of a-IGZO TFTs as a positive bias temperature stress (PBTS) time with (a) STD and (b) Split structures, respectively. The stress conditions of PBTS was V_{GS} = + 20 V at 60 ℃ for 1 h.

We investigated the electrical characteristics of the a-IGZO TFTs with the STD and Split structures as shown in Fig. 3(a) and 3(b), respectively. The drain currents of the Split TFTs are much higher than those of STD TFTs. The μ_{FE}'s are 17.2 and 77.9 cm^2/Vs at V_{GS} = 20 V for STD and Split TFTs, respectively. And, the E/S oxide TFT with split active layer exhibits the lower subthreshold swing (SS) of 77 mV/dec, and the V_{TH} of 0.2 V. This indicate very low density of SiO_2/a-IGZO interface traps. The high mobility and excellent stability are correlated the improvement of top interface by the metal-F bond formation by F plasma for E/S pattering and subsequent reduction in the interface state density [6].

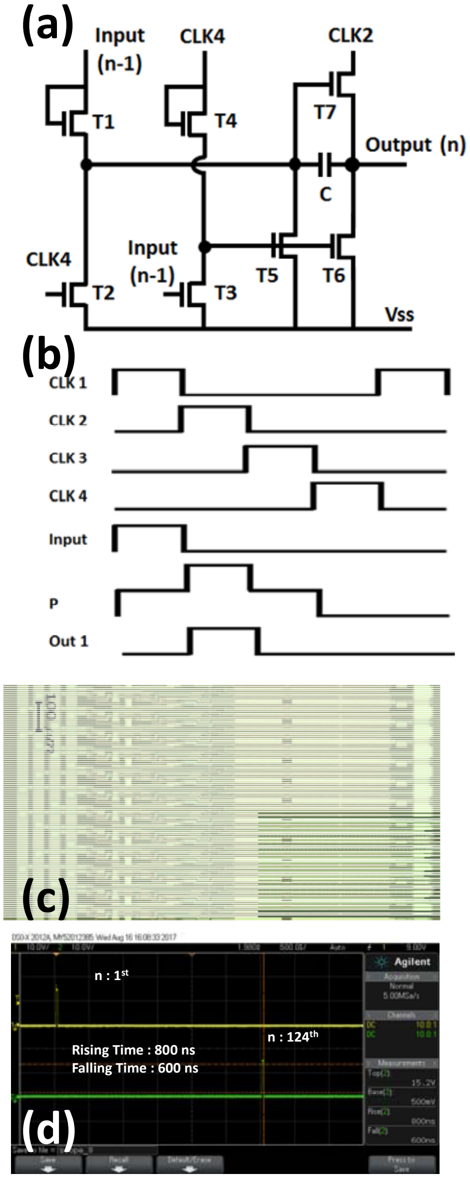

Figure 4. The gate driver with split active layer. (a) Equivalent circuit schematic, (b) timing diagram, (c) optical image of a 124 stage gate driver and (d) input signal and last stage (124th) output.

After positive bias temperature stress (PBTS), SS and V_{TH} increase with increasing stress time for a-IGZO TFT with STD structure, but a-IGZO TFT with Split structure has negligible change, as shown in Fig. 3(b). As a result, the a-IGZO TFT with Split active layer has very small ΔV_{TH} because of much less trap states at the gate insulator/active layer interface. Here, the excellent performance of a-IGZO TFT with split structures appear to be due to the improvement of the top interface by metal-F bonding.

The gate driver schematic design, timing diagram and optical image of integrated gate driver are depicted in Fig. 4(a), (b) and (c), respectively. A single stage of integrated gate driver consists of 7 TFTs and 1 bootstrap capacitor (7T1C). Each single stage consists of two output nodes. The additional output node is necessary to separate the output to the next stage from the panel to improve yield by reducing the influence of particles during the fabrication process, which may result in short or open in the gate/data lines and gate insulator/interlayer. The operational principle is similar to the one presented elsewhere [8]. The performance of 124-stages shift resistor with split structures, which functions well up to the last stage as shown in Fig.4(d) indicating Input signal and last stage (124th) output. The output voltage in the last stage, rise and fall times at V_{DD} = 15V are respectively, 800 ns and 600 ns.

The unique properties of oxide-based semiconductors such as wide bandgap and high transparency also make novel applications possible. For example, a see-through type transparent AMOLED can be realized using oxide based semiconductor.[9] Using such displays, one can see the objects in the opposite side of the displays, and thus many interesting applications can be possible. Since the transparency of such displays mostly relies on the use of transmission area and/or highly transparent materials. As shown in Fig. 5, we have successfully demonstrate a 4-inch QVGA (320×240) transparent AMOLED display based on IGZO TFTs with split active layer and transparent OLED.

The specifications of the prototype panel are described in Table. 1. The photograph of a transparent AMOLED display is shown in Fig. 5(a). Green monochrome, transparent AMOLED is designed with conventional two transistors and one capacitor (2T+1C) pixel structure. The 4-inch transparent display images taken from front and back sides are shown in Fig. 5(b) and (c), respectively.

4. Conclusion

We demonstrated a 4 inch transparent AMOLED display using a-IGZO TFT backplane with split active layer. The E/S IGZO TFTs with split active layer are used for AMOLED using conventional TFT process. The TFT device exhibits high performance with excellent stability under the PBTS. The μ_{FE} for a-IGZO TFTs with Split structures is 77.9 cm^2/Vs at V_{GS} = 15 V. And, the shift resistor exhibits excellent driving ability with its rising and falling times less than 1µs. The transparent AMOLED display based on oxide TFTs with split structures with integrated shift resistor are successfully demonstrated with OLED structure of an IZO/HAT-CN/NPB/TCTA/TCTA:TPBi: 12%Ir(ppy)$_3$/TPBi/LiF/Al/Ag. Therefore, the oxide TFT backplane with split active layer is suitable for high resolution, large area AMOLED displays

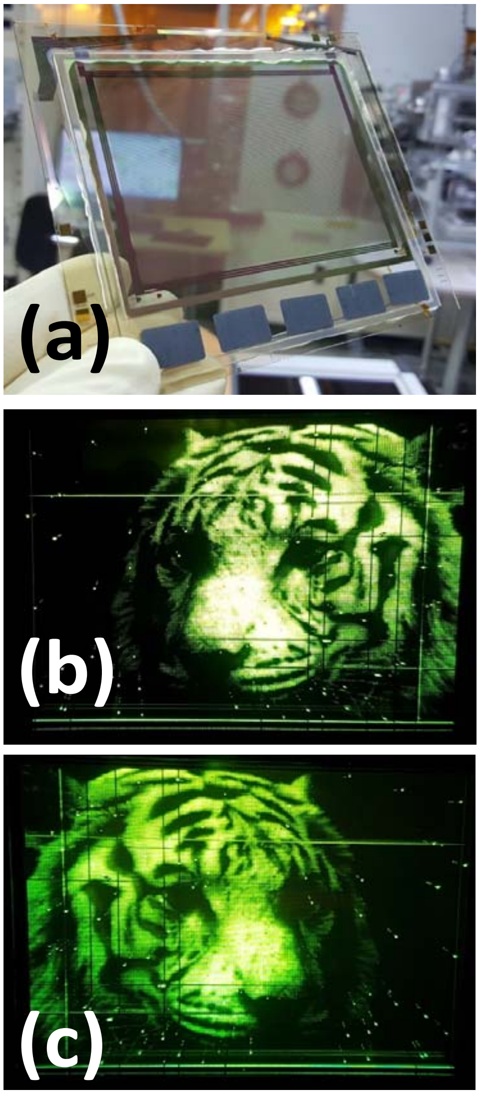

Figure 5. (a) A 4-inch transparent AMOLED display using the a-IGZO TFT backplane with split active layer showing transparent display. The 4-inch transparent display images taken from (b) front and (c) back sides.

Table 1. Specifications of the transparent AMOLED display

Specification	Data
Panel size	4-Inch
Pixel	QVGA (320 x 240)
Pixel circuit	2T1C
TFT driving mode	Split a-IGZO TFT
Aperture ratio (%)	45

5. Acknowledgements

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